

**WHAT IS CLAIMED IS:**

1        1. An integrated circuit receiving command information over a plurality  
2        of bit times, comprising:

3                a command queue storing command information received into the integrated  
4                circuit during consecutive bit times; and

5                control logic responsive to a cancellation indication in the command  
6                information, indicating that the command is canceled, to repoint a  
7                write pointer to point to the canceled command already stored in the  
8                command queue.

1        2. The integrated circuit as recited in claim 1 wherein the command is a  
2        speculative read operation.

1        3. The integrated circuit as recited in claim 1 wherein the command  
2        queue includes a plurality of FIFO buffers, each of the FIFO buffers storing a segment  
3        of a received command and wherein a plurality of write pointers point to locations in  
4        respective FIFO buffers to store a next command segment, and wherein segments of a  
5        command in different FIFO buffers are received at different bit times.

1        4. The integrated circuit as recited in claim 3 wherein a last FIFO storing  
2        a last command segment received during a last bit time for the command information  
3        is written to store a last portion of the command.

1        5. The integrated circuit as recited in claim 4 wherein the indication to  
2        cancel the current command is in the last command segment.

1        6. The integrated circuit as recited in claim 4 wherein each of the  
2        plurality of FIFOs has its respective write pointer decremented in consecutive clock  
3        intervals.

1        7. The integrated circuit as recited in claim 1 further comprising a content  
2        counter indicating a number of commands stored in the command buffer.

1        8.     The integrated circuit as recited in claim 7 wherein the content counter  
2 is decremented as a result of the cancellation indication.

1        9.     A method for storing command information into a command queue in  
2 an integrated circuit, comprising:

3                receiving a plurality of command segments corresponding to one command in  
4                a plurality of phases, each command segment being received in a  
5                different phase;  
6                pushing received command segments into a command queue;  
7                checking for a cancellation indication for the command being received;  
8                in response to the cancellation indication, performing an undo-push operation  
9                to remove the command segments stored in the command queue  
10              associated with the cancelled command.

1        10.    The method as recited in claim 9 wherein the command queue includes  
2 a plurality of FIFO buffers, each of the FIFO buffers storing respective command  
3 segments of a command received in a different bit time and wherein a plurality of  
4 write pointers point to locations in respective FIFO buffers to store a next command  
5 segment.

1        11.    The method as recited in claim 10 wherein the undo push operation  
2 includes decrementing the plurality of write pointers.

1        12.    The method as recited in claim 9 wherein further comprising writing a  
2 last command segment into a last FIFO buffer, the last command segment including  
3 the cancellation indication.

1        13.    The method as recited in claim 9 wherein the cancelled command is a  
2 speculative read command.

1        14.    The method as recited in claim 13 wherein the cancellation indication  
2 is a read valid bit indicating that the speculative read command is not valid.

1           15. The method as recited in claim 10 wherein the plurality of write  
2 pointers are decremented consecutively.

1           16. The method as recited in claim 15 wherein the undo push operation is  
2 started within one clock of receipt of the cancellation indication.

1           17. The method as recited in claim 9 further comprising maintaining a  
2 count of a number of commands currently in the command buffer.

1           18. The method as recited in claim 17 further comprising decrementing the  
2 count in response to the cancellation indication.

1           19. A computer system comprising:  
2           a processor;  
3           an integrated circuit coupled to receive a command from the processor over a  
4           command channel, the command being received in command segments  
5           corresponding at different times;  
6           a command queue in the integrated circuit coupled to receive the command  
7           segments;  
8           control logic coupled the command queue and responsive to a cancellation  
9           indication in one of the command segments indicative that a current  
10           command is canceled to perform an undo-push operation such that a  
11           next received command is placed in the command queue in a same  
12           location as the current command.

1           20. The computer system as recited in claim 19 wherein the integrated  
2 circuit includes a count of a number of commands in the command queue and wherein  
3 the count is decremented in response to the cancellation indication.